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EXAMINER	
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ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/825,694	HARPER ET AL.	
	Examiner	Art Unit	
	AARON M. GUERTIN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/02/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Claims 8-42 are presented for examination.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 12/02/2010 is being considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No.: US 2003/0011637 A1 (Boudier), in view of U.S. Publication No.: US 2002/0109682 (Nash) in further view of U.S. Publication No.: US 2005/0041031 A1 (Diard).

4. Regarding claim 8, Boudier teaches of a method of creating an image graph ([0092]), said image graph comprising one or more nodes ([Fig. 9, (910, 920, 950)]), inputs to those nodes, and outputs from those nodes (each node of Fig. 9 (900) is linked; also see [0054]-[0058]), the method comprising the steps of: the method comprising the steps of: **optimizing said image graph by running software on a**

CPU; compiling said image graph by running software on said CPU; (processor 504 is regarded as the CPU; the compiling is the optimization of the graph by executing the program(s) [0007], [0032], and [0037]); and **rendering said image graph by running said compiled image graph** ([0029]).

Boudier teaches the limitations of claim 8 above; however Boudier fails to specifically teach of **wherein the node(s) are program(s) and wherein executing the scene graph yielding a rendered image**.

Nash is analogous art that further teaches of **wherein the node(s) are program(s)** ([Fig. 3] and [0054]; furthermore [Fig. 6] shows phase modules (nodes) of processing and each node comprises a specific program code to conduct the function within said node in a sequence) **and wherein executing the modules yields a rendered image** ([0060], [0061] and [0062]).

All the elements of claim 8 are known in Boudier in view of Nash, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include wherein the nodes of Boudier are modules indicating a function that needs to be processed and wherein the execution of the modules renders an image in Boudier, as doing so would provide the means for effectively optimizing the calculations of the attributes to a specific image instead of only optimizing the steps of applying the attributes, reducing overall system calculations and increases system efficiency and bandwidth.

Boudier and Nash teach the limitations of claim 8 above; however, Boudier and Nash fail to specifically teach of wherein the **programs can be run on a GPU** (GPU programs) and therefore the compilation is conducted **on a GPU.**

Diard is analogous art that further teaches of wherein the **programs can be run on a GPU** (GPU programs) and therefore the compilation is conducted **on a GPU** ([0033]); and **utilizing a CPU and a graphics processing unit** ([0033] as disclosed above).

All the elements of claim 8 are known in Boudier and Nash in view of Diard, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include implementing the processing the compilation on a GPU wherein a combination of a CPU and GPU are used in Boudier, as doing so would provide the means and advantages of a higher throughput optimized, faster processing capabilities, and more advantageous memory bandwidth.

The combination of Boudier, Nash, and Diard from above, expressly teach **wherein the image graph comprises one or more GPU programs, inputs to the one or more GPU programs and outputs from the one or more GPU programs** (It was expressly taught by Boudier of completing an optimized scene graph wherein the graph was comprised of programs taught by Nash, Wherein the programs would be further executed within the hierarchy of programs in Boudier's scene graph to create an image which teaches "**representing, in memory, an image by an image graph"** ([0029]).

5. Regarding claim 9, Boudier, Nash, and Diard teach the limitations of claim 8 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches of **wherein the step of optimizing includes the step of using a cache look-up to see if said rendered image is already in cache** ([0094]).

6. Regarding claim 10, Boudier, Nash and Diard teach the limitations of claim 8 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches **wherein the step of optimizing includes the step of using a cache look-up to see if said image graph has already been optimized and is in a memory** (at step 630 the create optimization process executes and actually begins on step 710 wherein the memory is checked for a former optimized scene graph wherein upon extra parameters may be added if different from the existent optimization; and [Fig. 6] and [Fig. 7]; [0032], [0046]).

7. Regarding claim 11, Boudier, Nash and Diard teach the limitations of claim 8 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches **wherein the step of optimizing includes the step of calculating an intersection, said intersection representing an area where said rendered image is both defined by said image graph and part of a region requested by a process running on said CPU that has requested creation of said image** (NOTE: according to applicants specification [0089] - Core Imaging performs node reduction analysis and eliminates nodes where possible. After unnecessary (or collapsible) nodes are

optimized, Core Imaging moves to step 7103 where optimization is performed to ultimately limit the size of buffers and image inputs. This step involves intersecting two regions called domain of definition ("DOD") and region of interest ("ROI`). After the ROI/DOD optimization, the graph is ready to compile in step 7104… and [0111] - In developing optimization techniques, the domain of definition ("DOD") is interesting because there is no need to compute or draw pixels outside the DOD. Therefore, in optimizing a graph, there is use in first calculating the DOD of the root node (the very highest node, for example node 415 of FIG. 4).). From the disclosure in the specification and corresponding Fig. 4 and Fig. 7 for support of claim 11, it can be seen that the intersection is where two nodes come together as the optimization performs collapsing wherein each node then becomes a DOD and the result of the two nodes that intersect and come together at another node is a ROI.

Boudier optimizes in several ways encompassing the same method of the applicant. For example, as supported by Boudier in [0053] - [0059] are methods of "collapse geometers" and Collapse hierarchy which as supported by [Fig. 9] and [Fig. 10 and 11] optimizations are performed on DODs forming new DODs (if collapsing to the top of the scene graph then obtaining an ROI). ([Figs. 9-11] and [0054].) Furthermore as disclosed and incorporated by claim 8, the method of optimizing within intersections and regions is conducted on a processor (CPU).

8. Regarding claim 12, it is similar in scope to claim 8 and is rejected under the same rationale.

9. Regarding claim 13, it is similar in scope to claim 8 and is rejected under the same rationale.

10. Regarding claim 14, Boudier, Nash and Diard teach the limitations of claims 8 and 11 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches the step of, **using said calculated intersection to limit the number of pixels that require calculation during said rendering** (it is implied that an optimization by combining (collapsing) DODs that the scene graph no longer has to process each of the nodes, furthermore [0055], [Figs. 9-11], [0054]); and Diard further teaches as incorporated by claim 1 the rendering **on a GPU**.

11. Regarding claim 15, it is similar in scope to claim 14 and is rejected under the same rationale.

12. Regarding claim 16, it is similar in scope to claim 14 and is rejected under the same rationale.

13. Regarding claim 17, Boudier, Nash and Diard teach the limitations of claims 8 and 11 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches the step of, **using said calculated intersection to limit the amount of memory necessary for storing said rendered image** ([0059]).

14. Regarding claim 18, it is similar in scope to claim 17 and is rejected under the same rationale.

15. Regarding claim 19, it is similar in scope to claim 17 and is rejected under the same rationale.

16. Regarding claim 20, Boudier, Nash and Diard teach the limitations of claim 8 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches the step of wherein said step of optimizing comprises **the additional steps of using a cache to determine if said rendered image is available in memory** ([0094] as imported, the rationale disclosed in the rejection of claim 9); **using the CPU to perform region of interest (ROI) and domain of definition (DOD) intersections with respect to one or more of said nodes** (Boudier optimizes in several ways encompassing the same method of the applicant. For example, as supported by Boudier in [0053] - [0059] are methods of "collapse geometers" and Collapse hierarchy which as supported by [Fig. 9] and [Fig. 10 and 11] optimizations are performed on DODs forming new DODs (if collapsing to the top of the scene graph then obtaining an ROI). ([Figs. 9-11] and [0054]) Furthermore as disclosed and incorporated by claim 8, the method of optimizing within intersections and regions is conducted on a processor (CPU); **using the CPU to determine if nodes may be combined to form a node that has been created by combining two other nodes.** (Boudier by examples of [Fig. 12], [Fig. 13], and [Fig. 14] clearly show wherein the optimization programs (ability to

collapse) may be calculated to combine). Nash further teaches that the nodes are programs ([Figs. 3 and 6] and [0060] through [0062]).

Diard further teaches of **using a CPU to determine if said GPU is capable of performing** (by the feedback provided by the polling of the CPU to the GPU the indication that the GPU is capable of performing the task or if the task needs to be partitioned is complete and disclosed in [0050]).

17. Regarding claim 21, it is similar in scope to claim 20 and is rejected under the same rationale.

18. Regarding claim 22, it is similar in scope to claim 20 and is rejected under the same rationale.

19. Regarding claim 23, it is similar in scope to the combination of claims 8, 11, 14, 17, and 20 (the rationale disclosed in the rejection incorporated herein). However, claim 23 includes the additional limitations of a method for creating a rendered polygon, **receiving a request to render a polygon; creating a representation of said rendered polygon comprising a root GPU program and its relationship with other GPU programs, their inputs and outputs; calling the following groups of objects for each GPU program that must be run in order that the root GPU program may run to render said polygon; one or more objects for creating a buffer**.

Boudier teaches **receiving a request to render polygon; creating a representation of said rendered polygon comprising a root node and its**

relationship with other nodes, their inputs and outputs; calling the following groups of objects for each node that must be run in order that the root node may run to render said polygon; one or more objects for creating a buffer (the rendering of Boudier is created by creating a platform to optimize the processing and then executing the platform whereupon an image or objected is rendered, by the nature of rendering graphics is implied that polygons are rendered in order to create the make up of the object or image; [0005], [0006], and [0007]).

Nash is analogous art that further teaches of **wherein the node(s) are program(s)** ([Fig. 3] and [0054]; furthermore [Fig. 6] shows phase modules (nodes) of processing and each node comprises a specific program code to conduct the function within said node in a sequence) **and wherein executing the modules yields a rendered image** ([0060], [0061] and [0062]).

All the elements of claim 23 are known in Boudier in view of Nash, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include wherein the nodes of Boudier are modules indicating a function that needs to be processed and wherein the execution of the modules renders an image in Boudier, as doing so would provide the means for effectively optimizing the calculations of the attributes to a specific image instead of only optimizing the steps of applying the attributes, reducing overall system calculations and increases system efficiency and bandwidth.

Boudier and Nash teach the limitations of claim 8 above; however, Boudier and Nash fail to specifically teach of wherein the **programs can be run on a GPU** (GPU programs) and therefore the compilation is conducted **on a GPU.**

Diard is analogous art that further teaches of wherein the **programs can be run on a GPU** (GPU programs) and therefore the compilation is conducted **on a GPU** ([0033]).

All the elements of claim 23 are known in Boudier and Nash in view of Diard, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Boudier the implementation of processing the compilation on a GPU as suggested by Diard, as doing so would provide the means and advantages of a higher throughput optimized, faster processing capabilities, and more advantageous memory bandwidth.

20. Regarding claim 24, the rationale disclosed in claim 23 is incorporated herein.

21. Regarding claim 25, Boudier, Nash, and Diard teach the limitations of claim 23 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches **wherein said representation of said rendered polygon is a low-level graph** (the low level graph is disclosed by fig. 9 (left side) wherein it has not been collapsed).

22. Regarding claim 26, Boudier, Nash, and Diard teach the limitations of claim 23 above, the rationale disclosed in the rejection incorporated herein and Boudier further teaches **wherein said representation of said rendered polygon is a high-level graph** (the high level graph is disclosed by fig. 9 (right side) wherein it has been collapsed).

23. Regarding claim 27, the rationale disclosed in the rejection of claim 23 is incorporated herein.

24. Regarding claim 28, the rationale disclosed in the rejection of claim 23 is incorporated herein.

25. Regarding claim 29, the rationale disclosed in the rejection of claim 23 is incorporated herein.

26. Regarding claim 30, the rationale disclosed in the rejection of claim 23 is incorporated herein.

27. Regarding claim 31, it is similar in scope to claims 8 and 23; the rationale applied in the rejections of both claims 1 and 23 is incorporated herein.

28. Regarding claim 32, it is similar in scope to claim 25 and is rejected under the same rationale.

29. Regarding claim 33, it is similar in scope to claim 26 and is rejected under the same rationale.

30. Regarding claim 34, it is similar in scope to claim 23 and is rejected under the same rationale.

31. Regarding claim 35, it is similar in scope to claim 27 and is rejected under the same rationale.

32. Regarding claim 36, it is similar in scope to claim 28 and is rejected under the same rationale.

33. Regarding claim 37, it is similar in scope to claim 29 and is rejected under the same rationale.

34. Regarding claim 38, it is similar in scope to claim 30 and is rejected under the same rationale.

35. Regarding claim 39, it is similar in scope to claims 8, 23 or 31 (the rationale disclosed in the rejection incorporated herein. However, claim 39 includes the additional limitation of **providing a computer-readable medium with executable instructions**. Boudier further teaches of **providing a computer-readable medium with executable instructions** [0038]).

36. Regarding claim 40, it is similar in scope to claim 8 (the rationale disclosed in the rejection of claim 8 incorporated herein). Furthermore, claim 40 has the additional limitations of a system which include: **A computer system configured for creating an image, the computer system comprising: a central processing unit (CPU); a graphics processing unit (GPU) communicatively coupled to the CPU; and a**

memory communicatively coupled to the CPU and/or the GPU having, the memory storing computer executable instructions executable by the CPU and/or the GPU to configure the CPU and GPU. Boudier teaches of providing a computer-readable medium with executable instructions within a computer system [0038]). Nash is analogous art that further teaches of wherein the node(s) are program(s) ([Fig. 3] and [0054]; furthermore [Fig. 6] shows phase modules (nodes) of processing and each node comprises a specific program code to conduct the function within said node in a sequence) and wherein executing the modules yields a rendered image ([0060], [0061] and [0062] which show creating an image and Diard was incorporated in to claim 8 to teach the combination of hardware **a central processing unit (CPU)** ([Fig 1, (102)])**; a graphics processing unit (GPU) communicatively coupled to the CPU** ([Fig. 1, (114a-b)])**; and a memory communicatively coupled to the CPU and/or the GPU having** ([Fig. 1, (116a)] and see [0028] thru [0030] for explicit architecture)). The combination of Boudier, Nash, and Diard expressly teach the system with components wherein **the memory storing computer executable instructions executable by the CPU and/or the GPU to configure the CPU and GPU** (See all rationale of claim 8, incorporated herein to teach the memory, executable instructions and CPU/GPU structure of the system to operatively provide the method of claim 8).

37. Regarding claim 41, it is similar in scope to claim 23 (the rationale disclosed in the rejection of claim 23 incorporated herein). Furthermore, claim 41 has the additional limitations of a system which include: **A computer system configured for creating an**

image, the computer system comprising: a central processing unit (CPU); a graphics processing unit (GPU) communicatively coupled to the CPU; and a memory communicatively coupled to the CPU and/or the GPU having, the memory storing computer executable instructions executable by the CPU and/or the GPU to configure the CPU and GPU. Boudier teaches of providing a computer-readable medium with executable instructions within a computer system [0038]). Nash is analogous art that further teaches of wherein the node(s) are program(s) ([Fig. 3] and [0054]; furthermore [Fig. 6] shows phase modules (nodes) of processing and each node comprises a specific program code to conduct the function within said node in a sequence) and wherein executing the modules yields a rendered image ([0060], [0061] and [0062] which show creating an image and Diard was incorporated in to claim 8 to teach the combination of hardware **a central processing unit (CPU)** ([Fig 1, (102)])**; a graphics processing unit (GPU) communicatively coupled to the CPU** ([Fig. 1, (114a-b)])**; and a memory communicatively coupled to the CPU and/or the GPU having** ([Fig. 1, (116a)] and see [0028] thru [0030] for explicit architecture)). The combination of Boudier, Nash, and Diard expressly teach the system with components wherein **the memory storing computer executable instructions executable by the CPU and/or the GPU to configure the CPU and GPU** (See all rationale of claim 23, incorporated herein to teach the memory, executable instructions and CPU/GPU structure of the system to operatively provide the method of claim 23).

38. Regarding claim 42, it is similar in scope to claim 31 (the rationale disclosed in the rejection of claim 31 incorporated herein). Furthermore, claim 42 has the additional limitations of a system which include: **A computer system configured for creating an image, the computer system comprising: a central processing unit (CPU); a graphics processing unit (GPU) communicatively coupled to the CPU; and a memory communicatively coupled to the CPU and/or the GPU having, the memory storing computer executable instructions executable by the CPU and/or the GPU to configure the CPU and GPU**. Boudier teaches of providing a computer-readable medium with executable instructions within a computer system [0038]). Nash is analogous art that further teaches of wherein the node(s) are program(s) ([Fig. 3] and [0054]; furthermore [Fig. 6] shows phase modules (nodes) of processing and each node comprises a specific program code to conduct the function within said node in a sequence) and wherein executing the modules yields a rendered image ([0060], [0061] and [0062] which show creating an image and Diard was incorporated in to claim 8 to teach the combination of hardware **a central processing unit (CPU)** ([Fig 1, (102)])**; a graphics processing unit (GPU) communicatively coupled to the CPU** ([Fig. 1, (114a-b)])**; and a memory communicatively coupled to the CPU and/or the GPU having** ([Fig. 1, (116a)] and see [0028] thru [0030] for explicit architecture)). The combination of Boudier, Nash, and Diard expressly teach the system with components wherein **the memory storing computer executable instructions executable by the CPU and/or the GPU to configure the CPU and GPU** (See all rationale of claim 31,

incorporated herein to teach the memory, executable instructions and CPU/GPU structure of the system to operatively provide the method of claim 31).

Response to Arguments

39. NOTE: The above Office Action (OA) includes the exact same citations of prior art as previously sent within the Non Final OA mailed 9/2/2010 (The OA of 9/2/2010 may be referred to for rationale as it is the same but with more extensive citations; they are the same.). The only difference is the examiner removed the text corresponding with each of the citations as an attempt to clarify the content of the OA for the applicant. As the rejection is the same and there rejection is being maintained, this OA has been properly made Final. Please see the response to applicants remarks below for further detail.

[Summary of Telephone Conversation]

40. The Examiner also thanks the Applicant for taking the time to go through concerns with the application process of the instant application. All comments, remarks, arguments have been fully considered and as the claims are read on by prior art (despite the discrepancies within the previous response to arguments) the OA has been made final because no change in prior art was necessary to fully teach or suggest each and every limitation either solely or in combination of said prior art. All comments, remarks, arguments are further responded to as necessary below.

[Claim Rejections under 35 USC 103(a)]

41. Applicant's arguments, Remarks, Pages 10-12, in summary, appear to, recite that the applicant did not feel that the examiner addressed the amendment made on 9/2/2010.

The examiner respectfully disagrees. The examiner apologizes for any un-clear interpretation in the instant application, however, each and every limitation has been taught either solely or in combination by prior art of record. It is respectfully pointed out that the references of the prior art rejection in fact did teach the limitations presented in the preamble regardless of the patentable weight that was given. The only difference between the OA mailed with before the applicants amendment and after the applicants amendment was the location of the limitation. It was moved by the examiner with corresponding prior art teachings into the body of the claim, where the applicant had made said amendment. For example, within the OA above, each and every limitation, including the former amendment has been addressed and no change to the OA above has been made from the previous OA of 9/2/2010, therefore the amendment was considered and accounted for. To further clarify the portion of the OA the applicant cited, it was only to show how patentable weight is usually given. The Applicant should also notice that in said OA the examiner cited prior art within the preamble (which actually in every OA sent included citations disclosing how, if in the body of the claim, the language was read on by prior art.). Considering prior art has been cited in all OA's mailed for the limitations in the preamble before and after a portion of the language had been amended into the body of the claims, each limitation had been addressed by the

examiner within all OA, therefore, For at least the reasons above, the examiner will be maintaining the rejection and maintaining that the OA herein is being made Final (also please notice the examiner did expressly pages 5-7 of the OA of 9/2/2010 disclose teachings for the amended portion which was NOT disclosed in the same way in the OA mailed 11/04/2009 (OA before RCE) expressly showing the examiner did consider each and every limitation.).

[Claim 8]

42. Applicant's arguments, Remarks Pages 13-15, are directed to claim 8. Applicant's arguments are confusing, but the examiner will do as best to answer, it appears that the applicant, in summary, recites that the limitations of the independent claim have not been taught or suggested by prior art of record.

The Examiner respectfully disagrees. With respect to applicant's remarks on pg. 13, the applicant mentions that the graph of Boudier does not teach the graph of the instant application and that "Boudier does not have anything to do with programs and inputs/outputs to programs". The examiner respectfully points out that Boudier was the only reference relied upon for teaching the image graph. Boudier teaches of an image graph that is being optimized, wherein the optimization process can be performed for any of a number of purposes, such as the enhancement of scene graph traversal time, the enhancement of drawing time, the reduction of memory usage, improved efficiency of data manipulation, and the targeting of a specific rendering platform (abstract). The combination of Boudier and Nash expressly show that it would have been obvious for

one of ordinary skill in the art to use the nodes of Boudier as execution modules which therefore are optimized as Boudier teaches. Execution modules are known to be programs to one of ordinary skill in the art. Execution modules would inherently have at least one input and output, as without them, said execution module would be non functional. The OA expressly teaches the combination of Boudier, Nash and Diard which teach **wherein the image graph comprises one or more GPU programs, inputs to the one or more GPU programs and outputs from the one or more GPU programs.** Page 14 of the remarks is unclear to the examiner. The applicant appears to be confusing the combination of references and asserts that the examiner provides no support for the rationales. The examiner respectfully disagrees. Boudier teaches of a method of creating an image graph ([0092]), said image graph comprising one or more nodes ([Fig. 9, (910, 920, 950)]), inputs to those nodes, and outputs from those nodes (each node of Fig. 9 (900) is linked; also see [0054]-[0058]), the method comprising the steps of: the method comprising the steps of: optimizing said image graph by running software on a CPU; compiling said image graph by running software on said CPU; (processor 504 is regarded as the CPU; the compiling is the optimization of the graph by executing the program(s) [0007], [0032], and [0037]); and rendering said image graph by running said compiled image graph ([0029]). Nash is analogous art that further teaches of wherein the node(s) are program(s) ([Fig. 3] and [0054]; furthermore [Fig. 6] shows phase modules (nodes) of processing and each node comprises a specific program code to conduct the function within said node in a sequence) and wherein executing the modules yields a rendered image ([0060], [0061] and [0062]). The

examiner expressly supported the combination by the recitation that “it would have been obvious to one of ordinary skill in the art at the time of the invention to include wherein the nodes of Boudier are modules indicating a function that needs to be processed and wherein the execution of the modules renders an image in Boudier, as doing so would provide the means for effectively optimizing the calculations of the attributes to a specific image instead of only optimizing the steps of applying the attributes, reducing overall system calculations and increases system efficiency and bandwidth.” Boudier expressly states the advantages of optimization within the abstract and so supporting the very conclusory statement made by the examiner. Furthermore the examiner expressly showed how Diard is analogous art that further teaches of wherein the programs can be run on a GPU (GPU programs) and therefore the compilation is conducted on a GPU ([0033]); and utilizing a CPU and a graphics processing unit ([0033] as disclosed above) because it would have been obvious to one of ordinary skill in the art at the time of the invention to include implementing the processing the compilation on a GPU wherein a combination of a CPU and GPU are used in Boudier, as doing so would provide the means and advantages of a higher throughput optimized, faster processing capabilities, and more advantageous memory bandwidth. Lastly the combination of Boudier, Nash, and Diard from above, expressly teach wherein the image graph comprises one or more GPU programs, inputs to the one or more GPU programs and outputs from the one or more GPU programs (It was expressly taught by Boudier of completing an optimized scene graph wherein the graph was comprised of programs taught by Nash, Wherein the programs would be further executed within the

hierarchy of programs in Boudier's scene graph to create an image which teaches "representing, in memory, an image by an image graph" ([0029]). The Applicant asserts that the combination would be a substantial reconstruction; however the applicant has not shown how this could be. One of ordinary skill in the art understands the importance of optimization, to simply use an optimization method as Boudier shows on the physical execution programs would be obvious to one of ordinary skill in the art because Nash already attempts to optimize. The optimization is not in a tree structure or an image graph structure but to supplement a texture data for a program module would be practical and would have been motivated by the advantages listed above. In response to applicant's argument that there is no teaching, suggestion, or motivation to combine the references, the examiner recognizes that obviousness may be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), and *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007). In this case, the motivation has been clearly shown by all of the explanations above. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed

invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Considering each and every limitation has been disclosed, suggested, or taught either solely or in combination by prior art of record, a case of prima facie case of obviousness has been met and is correct, therefore the rejection of claim 8 for at least the reasons above has been maintained.

43. Claims 9-22 are either directly or indirectly dependent from independent claim 8, therefore the rejections of claims 9-22 are at least maintained for the deficiencies incorporated by the claim upon which it depends.

[Claim 23]

44. The Applicants arguments with respect to independent claim 23 are similar in scope to the arguments made for independent claim 8 above, wherein the applicant makes allegations that the prior art of record fails to teach each and every limitation. The examiner respectfully disagrees. For the same reason as above, the rejection of claim 23 has been maintained.

45. Claims 24-30 are either directly or indirectly dependent from independent claim 23, therefore the rejections of claims 24-30 are at least maintained for the deficiencies incorporated by the claim upon which it depends.

[Claim 31]

46. The Applicants arguments with respect to independent claim 31 are similar in scope to the arguments made for independent claims 8 and 23 above, wherein the applicant makes allegations that the prior art of record fails to teach each and every limitation. The examiner respectfully disagrees. For the same reason as above, the rejection of claim 31 has been maintained.

47. Claims 32-38 are either directly or indirectly dependent from independent claim 31, therefore the rejections of claims 32-38 are at least maintained for the deficiencies incorporated by the claim upon which it depends.

[Claim 39]

48. The Applicants arguments with respect to independent claim 39 are similar in scope to the arguments made for independent claims 8, 23, and 31 above, wherein the applicant makes allegations that the prior art of record fails to teach each and every limitation. The examiner respectfully disagrees as prior art has clearly been cited to show how each and every limitation had been obvious for one of ordinary skill in the art at the time of the invention. For the same reason as above, the rejection of claim 39 has been maintained.

[Claims 40-42]

49. The Applicants arguments with respect to independent claims 40-42 are similar in scope to the arguments made for independent claims 8, 23, and 31 above, wherein

the applicant makes allegations that the prior art of record fails to teach each and every limitation. The examiner respectfully disagrees as prior art has clearly been cited to show how each and every limitation had been obvious for one of ordinary skill in the art at the time of the invention. For the same reason as above, the rejection of claims 40-42 have been maintained.

Conclusion

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AARON M. GUERTIN whose telephone number is (571)270-1547. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. M. G./
Examiner, Art Unit 2629

/Alexander Eisen/
Supervisory Patent Examiner, Art Unit 2629